

Application No. 10/747,802
Filing Date: 12/29/2003
Attorney Docket No.: INTEL12

REMARKS

The undersigned attorney thanks Examiner Auduong for his careful review of this patent application. Prior to entry of this amendment, claims 1 - 44 were pending in the application. Claims 1, 6, 12, 17, and 23-44 have been amended. Upon entry of this amendment, claims 1 - 44 will be pending.

Claims 1 – 44 Are Allowable Over the Cited Reference

In paragraphs 1 and 2, the Office Action rejected claims 1 – 44 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,392,253 to Asumi et al. (hereinafter “*Asumi*”). The rejection is respectfully traversed.

Asumi describes a nonvolatile semiconductor memory device in which a negative voltage is applied to a gate electrode of a memory cell transistor during an erase mode. The memory device includes a row decoder circuit having an N-channel transistor connected to a word line. The N-channel transistor is provided on a P-type well region of a semiconductor substrate. A negative voltage is applied to the P-type well region during the erase mode, while ground potential is applied thereto during other modes. (*see Asumi abstract*)

Asumi does not describe providing a source of a limited current, a first semiconductor device for providing a level-shifted output signal and a second semiconductor device, the second semiconductor device being a low-voltage device.

The invention of Claim 1 of the present invention, describes a circuit with a current limiting device and a level-shifting semiconductor for providing a level-shifted output signal to a low-power semiconductor. The use of the current limiting device and the level-shifting semiconductor allow the use of low-power semiconductors in the circuit. Such low-power semiconductors are typically faster and smaller than high-power semiconductors.

Each and every element of the claimed invention must be found in the reference to establish a *prima facie* case of anticipation. MPEP §2131. *Asumi* does not describe, teach, or suggest, a circuit with a source of a limited current, (i.e., current limiting device), and a first semiconductor for providing a level-shifted output signal to a low-power semiconductor, as described by Claim 1. The Office Action states that the transistors 26 and 27 as described by

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Aisumi, are interpreted as meeting the limitations of the claim. Notably, it appears that the Office Action identifies transistor 26 as both the source of a limited current and the first semiconductor. The Applicant respectfully disagrees with this interpretation of *Aisumi*. Nonetheless, the Applicant has amended Claim 1 to clarify that the source of a limited current and the first semiconductor are two distinct elements. As amended, Claim 1 claims a source of a limited current connected between a power source and a first node; a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node to provide a level-shifted output signal at the first node; and a second semiconductor device, having an input connected to an input signal, and having an output connected to the second node, the second semiconductor being a low-voltage device. Thus, the connections of the source of a limited current and the first semiconductor clarify that they are two distinct elements connected in series.

Additionally, the Applicant respectfully submits that *Aisumi* does not teach, disclose or suggest the use of a second semiconductor that is a low-voltage device. Accordingly, *Aisumi* does not disclose, teach, or suggest each and every element of Claim 1 for the further reason that Claim 1 claims the use of a low-voltage second semiconductor.

Because the cited reference does not describe, teach, or suggest a source of limited current connected between a power source and a first node; a first semiconductor device having an input connected to a bias voltage, and being connected between the first node and a second node to provide a level-shifted output signal at the first node; and a second semiconductor device, having an input connected to an input signal, and having an output connected to the second node, the second semiconductor being a low-voltage device, it is respectfully submitted that Claim 1, and all claims that depend there from are patentable over the cited art and it is requested that the rejection be removed and the claims be allowed to issuance.

In the Office Action, the Examiner directed the description of the rejection to Claims 39 through 44. Although Applicant has focused the above discussion on Claim 1, the explanation of the patentability of Claim 1 is equally applicable to Claim 39 as the relevant limitations of Claim 1 are also present in Claim 39.

Additionally, the Office Action rejected Claims 40-44 as anticipated by *Aisumi*. Each of these rejections are based on the premise that transistor 26 of *Aisumi* is both the source of a limited current and the first semiconductor. As explained above, through the present

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amendment, the Applicant clarifies that the source of a limited current is not the same device as the first semiconductor. Accordingly, transistor 26 of *Atsumi* can not be both the source of a limited current and the first semiconductor and the Applicant respectfully submits that *Atsumi* does not describe, teach, or suggest each and every limitation of Claims 40-44.

Accordingly, since each of Claims 1-44 includes the above discussed elements, which are not present in *Atsumi*, the Applicant respectfully submits that each of Claims 1-44 are in condition for allowance for the reasons stated above and for the further limitations contained therein.

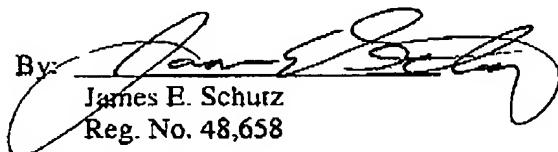
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CONCLUSION

It is respectfully submitted that claims 1 - 44 are in condition for allowance and that each point raised in the Official Action with regard to these claims has been fully addressed. Therefore, it is respectfully requested that the rejections to claims 1 - 44 be withdrawn and that claims 1 - 44 be processed to issuance in accordance with Patent Office Business.

If the Examiner believes that there are any issues that can be resolved by a telephone conference, or that there are any informalities that can be corrected by an Examiner's amendment, please contact Jim Schurtz at 404.885.3498.

Respectfully submitted,

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